(Currently amended) CLAIMS

What is claimed is:

1. (Currently amended) An integrated circuit package comprising:

a semiconductor die of plural separate power supply voltage domains; and

a switch mode DC-to-DC converter, ~~including at least:~~

wherein said switch mode DC-to-DC converter comprises:

an inductor core and windings;

a power switching transistor; and~~:~~

an ~~a digital open loop~~ output voltage fixing circuit comprising digital open-loop means requiring no feed-forward loop and no feedback loop.

2. (Canceled)

3. (Canceled)

4. (Previously Presented) An integrated circuit package comprising:

a semiconductor die of plural separate power supply voltage domains; and

a switch mode DC-to-DC converter,

wherein said switch mode DC-to-DC converter comprises:

an inductor core and windings;

a power switching transistor; and

an output voltage fixing circuit,

~~The integrated circuit of claim 1~~ wherein said semiconductor die comprises a decoder that compares an entry from a table corresponding to the present power state of said semiconductor die to a clock counter frequency divider output to determine duty cycle and/or switching frequency of said power switching transistor for said output voltage fixing circuit.

5. (Previously Presented) The integrated circuit of claim 4, wherein said table of entries of clock counter values to determine duty cycle is encoded within logic within said semiconductor die.

6. (Previously Presented) The integrated circuit of claim 4, wherein said table of entries of clock counter values to determine duty cycle is contained within non-volatile memory.

7. (Previously Presented) The integrated circuit package of claim ~~1~~ 4, wherein the power transistor gate-driving signal output from said semiconductor die is connected through a charge pump circuit to optimize efficiency of the power switching transistor of said DC-to-DC converter.

8. (Previously Presented) The integrated circuit package of claim ~~1~~ 4, ~~also~~ further comprising a substrate of fiberglass resin epoxy of type FR4 based laminate material for mounting said DC-to-DC converter components.

9. (Previously Presented) The integrated circuit package of claim 8, wherein said semiconductor die ~~contains~~ further comprises a plurality of pads from which to accept a binary number offset for fine tuning ~~the~~ said duty cycle and/or switching frequency by modifying the value compared to the clock counter frequency divider in said output voltage fixing circuit of said DC-to-DC converter.

10. (Previously Presented) The output voltage fixing circuit of claim 9, wherein said binary number offset is embodied within fusible leads on ~~the~~ said substrate that are electrically or mechanically trimmed or laser-trimmed at the factory.

11. (Previously Presented) The output voltage fixing circuit of claim 9, wherein said binary number offset is embodied within a wire-bonding option during assembly of said semiconductor die pads to the lead frame of said integrated circuit package.

12. (Previously Presented) The integrated circuit package of claim 8, wherein the power transistor gate driving signal output from said semiconductor die is connected through a trimmed delay circuit to fine tune the duty cycle of pulse width modulator or pulse frequency modulator of the output voltage fixing circuit of said DC-to-DC converter.

13. (Previously Presented) The output voltage fixing circuit of claim 12, wherein said trimmed delay circuit further comprises a printed film resistor on the substrate that is laser-trimmed at the factory.

14. (Currently amended) An integrated circuit package comprising: a substrate of fiberglass resin epoxy of type FR4 based laminate material for mounting:

a semiconductor die of plural separate power supply voltage domains; and

a switch mode DC-to-DC converter ~~including at least~~ further comprising an inductor core and windings, a power switching transistor, and ~~an a digital open-loop~~ output voltage fixing circuit comprising digital open-loop means requiring no feed-forward loop and no feedback loop.

15. (Previously Presented) The output voltage fixing circuit of claim 9, wherein said binary number offset is embodied within a wire-bonding option during assembly of said semiconductor die pads ~~to said substrate of claim 14~~ onto a substrate of fiberglass resin epoxy of type FR4 based laminate material.

16. (Previously Presented) A method for design and fabrication of an integrated circuit package comprising a semiconductor die of plural separate power supply voltage domains with an integrated switch mode power supply, said method comprising steps of:

designing a semi-custom or standard cell library based digital core and obtaining from the design automation tools power consumption estimates in various power states given known clocking rates;

determining switch mode power supply frequency, inductance, and duty cycles for various power states given ~~the above~~ said power consumption estimates and system clocking;

fabricating said semiconductor die for prototyping purposes, packaged without said integrated switch mode power supply;

characterizing said prototype semiconductor die for power consumption over all operating power states and environmental conditions and process variations;

fabricating said switch mode power supply onto final production substrates;

trimming the output voltage fixing circuit of said switch mode power supply after a probe test to determine the output voltages at given duty cycles versus output currents defined by ~~the~~ said semiconductor die known characterization data;

bonding and molding or sealing with epoxy said semiconductor die and power supply substrate into an integrated package.

17. (Previously Presented) The method of claim 16, wherein said step of trimming the output voltage fixing circuit further comprises a ~~further~~ step of binning said final production power supply substrates into the appropriate wire-bonding assembly line to set the proper binary number offset of the output voltage fixing circuit.

18. (Previously Presented) The method of claim 16, wherein said step of trimming the output voltage fixing circuit further comprises a ~~further~~ step of breaking fusible leads on said final production power supply substrate to set the binary number offset of the output voltage fixing circuit.

19. (Previously Presented) The method of claim 16, wherein said step of trimming the output voltage fixing circuit further comprises a ~~further~~ step of laser trimming a printed film resistor forming a delay circuit of the output voltage fixing circuit on said final power supply substrate.

20. (Previously Presented) The method of claim 16, wherein said step of trimming the output voltage fixing circuit further comprises a ~~further~~ step of programming a non-volatile memory with entries of clock counter values to determine duty cycle and/or switching frequency corresponding to each power state of the semiconductor die.

21. (Previously Presented) A method for design and fabrication of an integrated circuit package comprising a semiconductor die of plural separate power supply voltage domains with an integrated switch mode power supply, said method comprising steps of:

designing a semi-custom or standard cell library based digital core and obtaining from the design automation tools power consumption estimates in various power states given known clocking rates;

determining switch mode power supply frequency, inductance, and duty cycles for various power states given ~~above~~ said power consumption estimates and system clocking;

fabricating said semiconductor die for prototyping purposes, packaged without said integrated switch mode power supply;

characterizing said prototype semiconductor die for power consumption over all operating power states and environmental conditions and process variations;

fabricating said switch mode power supply onto final production substrates;

bonding and molding or sealing with epoxy said semiconductor die and assembled final power supply substrate into an integrated package.